

## ABSTRACT OF THE DISCLOSURE

METHOD AND SYSTEM FOR DETERMINING AN INTERCONNECT DELAY  
UTILIZING AN EFFECTIVE CAPACITANCE METRIC (ECM)  
SIGNAL DELAY MODEL

A method for determining an interconnect delay at a node in an interconnect having a plurality of nodes. The method includes performing a bottom-up tree traversal to compute the first three admittance moments for each of the nodes in the interconnect. The computed admittance moments are utilized, in an advantageous embodiment, to compute a p-model of the downstream load. Next, the equivalent effective capacitance value  $C_{eff}$  is computed utilizing the components of the computed pi-model and the Elmore delay at the node under evaluation. In an advantageous embodiment,  $C_{eff}$  is characterized by:

$$C_{eff} = C_{fj} (1 - e^{-T/\tau_{dj}})$$

where  $C_{fj}$  is the far-end capacitance of the pi-model at the node,  $T$  is the Elmore delay at the node and  $\tau_{dj}$  is the resistance of the pi-model ( $R_{dj}$ ) multiplied by  $C_{fi}$ . The interconnect delay at the node is then determined utilizing an effective capacitance metric (ECM) delay model characterized by:

$$ECM_j = ECM_{p(j)} + R_j (C_j + C_{nj} + C_{eff})$$

where  $ECM_{p(j)}$  is the computed ECM delay at the node immediately preceding the node under evaluation,  $R_j$  is the resistance between the node under evaluation and the

35

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